REMARKS

The Applicants request reconsideration of the rejection.

Claims 1-44, and 50-52 are pending.

A new title has been provided as required by the Examiner.

Claims 1-13, 22-35, and 51 were rejected under 35 USC §103 as being unpatentable over Roy, U.S. 6,499,121 (Roy) in view of Momohara, U.S. 6,094,733 (Momohara). The Applicants traverse as follows.

Each of the rejected independent claims recites a step of supplying a memory device to be tested with at least one signal that is also supplied to a memory device of a data processing unit, and a step of checking a relationship between output signals produced from these two memory devices. As a consequence of these two steps, the inventive method is used to confirm the operating reliability of the memory device to be tested, using the memory device of the data processing unit as a reference.

Parenthetically, although the claims have been amended for clarity and consistency of terms, no amendment has been made for patentability purposes or to narrow any claim.

The primary reference to Roy describes an interface circuit 226 which drives a combination of inputs and monitors a combination of outputs of one or more devices under test (DUTs). More specifically, subcircuits 216 of the interface

circuit read data from addresses provided by a tester 108 and compare the data with data also provided by the tester 108.

The secondary reference to Momohara discloses a method and apparatus for testing memory devices in which multiple function tests, a DC characteristic test and a redundancy analysis are performed for a DUT in parallel.

Neither Roy or Momohara, however, discloses the testing of the two memory devices as claimed using the same signal in order to test a memory device in quasi-operating conditions. More specifically, neither reference nor discloses to supply a memory device to be tested with a signal supplied to a memory device mounted on a data processing unit, and a step of checking a relationship between output signals from these two memory devices as a method of testing the memory device to be tested. Therefore, the combination of teachings of these two documents cannot be said to render obvious the claimed invention.

Claim 50 was rejected under 35 U.S.C. §102(e) as being anticipated by LeBlanc et al., U.S. 6,055,653 (LeBlanc). However, whereas LeBlanc discloses a method and apparatus for testing gang memory modules in which output data from a known good SIMM or DIMM an output data from a SIMM or DIMM are compared and any difference displayed to identify errors. However, LeBlanc does not show a test method in which a memory device to be tested is provided with a signal supplied to a

memory device mounted on a data processing unit, and a step of checking a relationship between output signals produced from these two memory devices.

In view of the foregoing amendments and remarks, reconsideration and reexamination are respectfully requested.

Respectfully submitted,

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